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Partho Pratim Mishra, Hemant Kanakia, Satish K. Tripathi

 April 1996 **IEEE/ACM Transactions on Networking (TON)**, Volume 4 Issue 2

 Full text available:  [pdf\(1.51 MB\)](#) Additional Information: [full citation](#), [references](#), [index terms](#)

**162** [A model of computation for VLSI with related complexity results](#)

Bernard Chazelle, Louis Monier

 May 1981 **Proceedings of the thirteenth annual ACM symposium on Theory of computing**

 Full text available:  [pdf\(677.06 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We propose a new model of computation for VLSI which is a refinement of previous models and makes the additional assumption that the time for propagating information is linear in the distance. Our approach is motivated by the failure of previous models to allow for realistic asymptotic analysis. While accommodating for basic laws of physics, this model tries to be most general and technology-independent. Thus, from a complexity viewpoint, it is especially suited for deriving lower ...

**163** [Reconfigurable computing: a survey of systems and software](#)

Katherine Compton, Scott Hauck

 June 2002 **ACM Computing Surveys (CSUR)**, Volume 34 Issue 2

 Full text available:  [pdf\(710.66 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

Due to its potential to greatly accelerate a wide variety of applications, reconfigurable computing has become a subject of a great deal of research. Its key feature is the ability to perform computations in hardware to increase performance, while retaining much of the flexibility of a software solution. In this survey, we explore the hardware aspects of reconfigurable computing machines, from single chip architectures to multi-chip systems, including internal structures and external coupling. W ...

**Keywords:** Automatic design, FPGA, field-programmable, manual design, reconfigurable architectures, reconfigurable computing, reconfigurable systems

**164** [Some compact layouts of the butterfly](#)

Yefim Dinitz, Shimon Even, Roni Kupersholt, Maria Zapolotsky


 June 1999 **Proceedings of the eleventh annual ACM symposium on Parallel algorithms and architectures**

 Full text available:  [pdf\(1.03 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)


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George Broomell, J. Robert Heath

June 1983 **ACM Computing Surveys (CSUR)**, Volume 15 Issue 2

Full text available: [pdf\(2.55 MB\)](#)

Additional Information: [full citation](#), [references](#), [citations](#)

**2** [The family of concurrent logic programming languages](#)

Ehud Shapiro

September 1989 **ACM Computing Surveys (CSUR)**, Volume 21 Issue 3

Full text available: [pdf\(9.62 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


Concurrent logic languages are high-level programming languages for parallel and distributed systems that offer a wide range of both known and novel concurrent programming techniques. Being logic programming languages, they preserve many advantages of the abstract logic programming model, including the logical reading of programs and computations, the convenience of representing data structures with logical terms and manipulating them using unification, and the amenability to metaprogrammin ...

**3** [Computer Communication Networks: Approaches, Objectives, and Performance Considerations](#)

Stephen R. Kimbleton, G. Michael Schneider

September 1975 **ACM Computing Surveys (CSUR)**, Volume 7 Issue 3

Full text available: [pdf\(3.99 MB\)](#)

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**4** [Session 1A: Dynamic verification: Static scheduling of multi-domain memories for functional verification](#)

Murali Kudlugi, Charles Selvidge, Russell Tessier

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: [pdf\(113.07 KB\)](#)

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Over the past decade both the quantity and complexity of available on-chip memory resources have increased dramatically. In order to ensure accurate ASIC behavior, both logic functions and memory resources must be successfully verified before fabrication. Often, the functional verification of contemporary ASIC memory is complicated by the presence of multiple design clocks that operate asynchronously to each other. The presence of multiple clock domains presents significant challenges for large ...

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John Colter, Netscape Navigator

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